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EXAMINER	
TRAN, VINCENT HUY	

ART UNIT	PAPER NUMBER
2115	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/753,032	WILSON, THOMAS J.	
	Examiner	Art Unit	
	Vincent T. Tran	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,8,12-16,20-35,37-42,44-47,49-54 and 56-70* is/are rejected.

7)☒ Claim(s) *5,6,9-11,17-19,36,43,48 and 55* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is responsive to the communication filed on 3/05/07 and 5/11/07

2. Claims 1-70 are pending for examination.

3. The text of those sections of Title 35, U.S. code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 20, 22-24, 28, 30-31, 59 are rejected under 35 U.S.C. 102(a) as being anticipated by Hall et al. US 20040213324 ("Hall").

6. As per claim 20, Hall discloses a machine implemented method to control a frequency of a clock signal generated by a phase locked loop (PLL) [fig. 15], the method comprising:

in response to a change in nominal frequency [paragraph 0077], obtaining profile address information which specifies a location of a profile stored in profile memory [15 fig. 15; paragraph 0079]; and

reading, form the profile memory according to the profile address information, profile data of the profile in sequence to control the PLL [paragraph 0080].

7. As per claim 22, Hall discloses the profile memory comprises RAM [paragraph 0079].

8. As per claim 23, Hall discloses the clock signal is spread spectrum modulated according to the profile data [paragraph 0080].

9. As per claim 24, Hall discloses the address information is obtained from the profile memory [paragraph 0079].

10. As per claim 28, Hall discloses a clock circuit for a data processing system, the circuit comprising:

a phase locked loop [fig. 15] to generate a clock signal, the PLL capable of adjusting the clock signal frequency among a plurality of nominal frequencies [fig. 1-14];

means for obtaining profile address information which specifies a location of a profile stored in profile memory, the profile corresponding to a nominal frequency [paragraph 0079]; and

means for reading, from the profile memory according to the profile address information, profile data of the profile in sequence to control the PLL to adjust a nominal frequency of the clock signal [paragraph 0080].

11. As per claim 30 and 31, see discussion in claim 22-23.

12. As per claim 59, Hall discloses a data processing system, comprising:

a phase locked loop (PLL) to generate a clock signal [fig. 15];

means for dynamically switching form using a first profile stored in profile memory to using a second profile stored in the profile memory for spread spectrum modulation of the clock signal through the PLL in response to a change in clock signal form a first nominal frequency to a second nominal frequency [paragraph 0077, 0079-0080; 0082].

13. Claims 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Endo et al. U.S. Patent No. 6,650,193 ("Endo").

14. As per claim 28, Endo discloses a clock circuit [10 fig. 1] for a data processing system, the circuit comprising:

a phase locked loop [50 fig. 1] to generate a clock signal, the PLL capable of adjusting the clock signal frequency among a plurality of nominal frequencies [inherent];

means for obtaining profile address information which specifies a location of a profile stored in profile memory, the profile corresponding to a nominal frequency [S15 fig. 9; col. 7 lines 15-30]; and

means for reading, from the profile memory according to the profile address information, profile data of the profile in sequence to control the PLL to adjust a nominal frequency of the clock signal [col. 8 lines 4-28].

15. Claims 20, 28, 59-61 are rejected under 35 U.S.C. 102(e) as being anticipated by Sha et al. U.S. Patent No. 6,980,581 ("Sha").

16. As per claim 28 and 20, Sha discloses a clock circuit [10 fig. 1] for a data processing system, the circuit comprising:

a phase locked loop [10 fig. 1] to generate a clock signal, the PLL capable of adjusting the clock signal frequency among a plurality of nominal frequencies [Fig. 3a-d];

means [22 fig. 1] for obtaining profile address information which specifies a location of a profile stored in profile memory [24 fig. 1], the profile corresponding to a nominal frequency [col. 2 lines 9-16]; and

means for reading, from the profile memory according to the profile address information, profile data of the profile in sequence to control the PLL to adjust a nominal frequency of the clock signal [see fig. 3a-d].

17. As per claim 59, Sha teaches a data processing system, comprising:

a phase locked loop to generate a clock signal [fig. 1].

means [20 Feedback Divider and 22 of fig. 1] for dynamically switching from using a first profile stored in profile memory to using second profile stored in the profile memory [24 ROM – inherent as discloses in 11-14][1] for spread spectrum modulation of the clock signal through the PLL in response [Feedback] to a change in clock signal from a first nominal frequency to a second nominal frequency [fig. 3a to 3d].

[1] Sha teaches, for good performance, a conventional spread spectrum clock generator requires a separate set of profile for each frequency at which the spread spectrum clock generator will operate. Therefore, in order to prevent the degradation of the spread spectrum modulation of the signal OUT as the PLL changes its frequency [show in fig. 3a-d], the system must able to dynamically switch [response to feedback 20] to another profile.

18. As per claim 61, Sha teaches means [24 fig. 1] for loading a plurality of profiles into the profile memory, the plurality of profiles comprising the first profile and the second profile.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

21. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

22. Claims 1-3, 7-8, 12-16, 20, 25-27, 32-35, 37-42, 44-47, 49-54, 56-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sha in view of Endo.

23. As per claim 1, Sha teaches a clock circuit for a data processing system, the circuit comprising:

a phase locked loop to generate a clock signal through phase locking to a reference signal [10 fig. 1];

profile memory [24 fig. 1] to store profile data comprising a plurality of entries; and

a profile state machine [22 fig. 1] couple to the profile memory and the PLL, the profile state read the profile data in sequence from the profile memory and to control the PLL to adjust a frequency of the clock signal according to the profile data read in sequence form the profile memory [col. 2 lines 9-14; 30-46];

where a number of entries of a profile read by the profile state machine in sequence to control the PLL is adjustable [inherent].

Sha fails to teach the profile memory capable of being updated in response to changes in nominal system frequency while the PLL generating the clock signal. The Sha's system is inefficient due to the fact the Sha's system required a large amounts of memory space to store the multiple set of profile for each different frequency.

Endo presents another invention relates to a clock circuit with a noise reduction function that reduces the EMI noise of electronic equipment wherein the circuit comprising an oscillation means that outputs the first reference signal, a memory means where modulation data for performing the spread spectrum modulation are selectively memorized, a write control means that performs writing of the modulation data to the memory means where the setting of the spread spectrum modulation memorized in the memory means can be updated [col. 2 lines 21-63]. Specifically, Sha teaches the profile memory [80 fig. 1] to store profile data capable of being updated while the PLL generating the clock signal [*S1 fig. 1 – a specific frequency is selected; S2 – the control unit updates the profile memory by search for information stored in HDD 155 (see fig. 4 and 5) and writes to the profile memory*].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the system of Sha with a profile memory capable of being update of Endo. The motivation for doing so would have been to provide Sha's clock circuit the ability to get the best EMI reduction without having to stored a large set of profile.

24. As per claim 2, Endo teaches the profile memory is a programmable memory [col. 5 lines 9-10].

25. As per claim 3, Sha teaches the profile state machine spread spectrum modulates the clock signal according to the plurality of entries [see fig. 3a-d].

26. As per claim 7, Sha teaches the profile memory is capable of simultaneously storing a plurality of profiles [col. 2 lines 25-30]; and, the profile state machine is capable of being instructed to used one of the plurality of profiles to control the PLL [inherent see claim 59 above].

27. As per claim 8, Sha inherently teaches the profile memory stores address information for accessing the plurality of profiles at predetermined location.

28. As per claim 12, see discussion in claim 1 and 7.

29. As per claim 13-14, see discussion in claim 2 and 3.

30. As per claim 15, see discussion in claim 8.

31. As per claim 16, Sha teaches the clock circuit is disposed on an IC chip [inherent – fig. 1].

32. As per claim 25, see discussion in claim 1.

33. As per claim 26, Sha teaches slewing the clock signal from a first nominal frequency to a second nominal frequency [from 3b to 3a where the nominal frequency slew from 78 MHz to 49 MHz; col. 2 lines 30-46];

wherein the profile data of the profile is read in sequence to spread spectrum modulate the clock signal when the clock signal in the second nominal frequency [*inherent since Sha teaches different profile is required for a particular nominal frequency else the effectiveness of spread spectrum modulation is compromise as frequency changes – col. 2 lines 9-30*].

34. As per claim 27, The examiner takes Official Notice that these are merely convention technique for power reduction.

35. As per claim 32, see discussion in claim 1.

36. As per claim 33, see discussion in claim 26.

37. As per claim 34, see discussion in claim 27.

38. As per claim 35, Sha teaches a machine implemented method to control a frequency of a clock signal generated by a phase locked loop, the method comprising:

dynamically, switching from using a first profile stored in profile memory to using a second profile stored in the profile memory for spread spectrum modulation of the clock signal

in response to a change in clock signal from a first nominal frequency to a second nominal frequency [*Figs 3a-3d traces the spread spectrum modulation of the signal OUT for each profile as the frequency of the signal OUT changes*].

And Endo teaches the profile memory is capable of being updated while the PLL generating the clock signal [see claim 1].

39. As per claim 37, Sha teaches loading the plurality of profiles into the profile memory, the plurality of profiles comprising the first profile and the second profile [col. 2 lines 25-29].

40. As per claim 38, Endo teaches replacing the first profile with a third profile in the profile memory [col. 5 lines 34-47].

41. As per claim 39, inherent.

42. As per claim 40, Sha teaches switching form using the second profile to using the third profile stored in profile memory for spread spectrum modulation of the clock signal [col. 2 lines 30-46].

43. As per claim 41 and 42, see discussion in claim 33.

44. As per claim 44, see discussion in claim 34.

45. As per claim 45 and 46, The examiner takes Official Notice that these are merely convention technique for power reduction and system protection.

46. As per claim 49-54, see discussion in claim 37-42.

47. As per claim 56-58, see discussion in claim 44-46.

48. Claims 21, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sha/Endo as applied to claim 20 or 28 above.

49. As per claim 21, The examiner takes Official Notice that these are merely convention technique to monitor the availability of the memory. Sha taught a system where the memory may including two or more spread profiles [col. 2 lines 25-30]. Therefore, one of ordinary skill in the art would be motivate to modify Sha's system with the means to indicate a size of each profile in order to prevent memory overflow.

50. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clementi U.S. Patent No. 6,294,936 in view of Endo.

51. As per claim 1, Clementi teaches a clock circuit [12 fig. 1] for a data processing system, the circuit comprising:

a phase locked loop [fig. 2] to generate a clock signal through phase locking to a reference signal [22 fig. 2];

profile memory [38 fig. 2] to store profile data comprising a plurality of entries; and

a profile state machine [26 fig. 2] couple to the profile memory and the PLL, the profile state read the profile data in sequence from the profile memory and to control the PLL to adjust a frequency of the clock signal according to the profile data read in sequence form the profile memory [col. 6 lines 10-34];

where a number of entries of a profile read by the profile state machine in sequence to control the PLL is adjustable [col. 6 lines 15-21].

Although Clementi teaches the profile memory is a programmable memory capable of being update to store any desire modulation waveform [col. 6 lines 50-53]. However, Clementi does not explicitly teach the profile memory capable of being updated while the PLL generating the clock signal.

Endo presents another invention relates to a clock circuit with a noise reduction function that reduces the EMI noise of electronic equipment wherein the circuit comprising an oscillation means that outputs the first reference signal, a memory means where modulation data for performing the spread spectrum modulation are selectively memorized, a write control means that performs writing of the modulation data to the memory means where the setting of the spread spectrum modulation memorized in the memory means can be updated [col. 2 lines 21-63]. Specifically, Sha teaches the profile memory [80 fig. 1] to store profile data capable of being updated while the PLL generating the clock signal [*S1 fig. 1 – a specific frequency is selected; S2 – the control unit updates the profile memory by search for information stored in HDD 155 (see fig. 4 and 5) and writes to the profile memory*].

At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the circuit of Clementi with a profile memory capable of being update while the PLL generating the clock signal of Endo. The motivation for doing so would have been to provide Clementi's clock circuit the ability to get the best EMI reduction without having to utilize a large memory for storing the multiple set of profile.

52. As per claim 2, Clementi teaches the profile memory is a programmable memory [col. 6 lines 50-53].

53. As per claim 3, Clementi teaches the profile state machine spread spectrum modulates the clock signal according to the plurality of entries [col. 6 lines 21-34].

54. As per claim 4, Clementi teaches a position of the profile in the profile memory, read by the profile state machine in sequence to control the PLL, is adjustable [col. 6 lines 10-20; 50-53].

55. Claims 60, 65-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sha as applied to claim 59 above, and further in view of Parikh U.S. Patent No. 7,061,331.

56. As per claim 60, Sha teaches means for loading a plurality of profiles into the profile memory, the plurality of profiles comprises the first profile, the second profile and a third profile [col. 2 lines 9-14];

means for spread spectrum modulation the clock signal at first nominal frequency using the first profile;

means for spread spectrum modulation the clock signal at the second nominal frequency using the third profile [inherent as discussion in claim 59].

Sha does not teach slewing the clock signal from the first nominal frequency to a second nominal frequency using the second profile.

Parikh teaches another method relates generally to electronic systems, and more particularly, to clock generation in electronic system. Specifically, Parikh teaches one technique

used to save power is to have clock generation circuit capable of producing multiple clock frequency; however, many clock generation circuit can become unstable during transitions between clock frequency. Consequently, the clock signal of such a clock generation circuit is generally turned off for a certain time period after a transition between clock frequencies [col. 1 lines 30-40]. Thus, Parikh teaches an invention directed to the use of a profile for slewing the clock signal from the first nominal frequency to a second nominal frequency [col. 4 lines 4-15, 39-45; fig. 2].

Therefore, at the time of the invention was made, it would have been obvious to one of ordinary skill in the art to have modified the circuit of Sha with a profile for slewing the clock frequency of a clock signal as taught by Parikh for the reason discussed above.

57. As per claim 65, Sha teaches the first profile is used to spread spectrum modulation of the clock signal when the clock signal has the first nominal frequency.

Parikh teach the used of another profile to slew the clock frequency from a first nominal frequency to a second nominal frequency.

58. As per claim 66, Sha inherently teach the second profile is used for spread spectrum modulation of the clock signal when the clock signal has the second nominal frequency.

59. As per claim 67, Parikh teaches the second profile is used to slew the clock signal from the first nominal frequency to the second nominal frequency.

60. As per claim 68, Parikh teaches the first nominal frequency is higher than the second nominal frequency; and the clock frequency is slewed from the first nominal frequency the second nominal frequency in response to a determination to reduce power consumption [col. 1 lines 30-35].

61. As per claim 69 – 70, The examiner takes Official Notice that these are merely convention technique for power reduction and system protection.

62. Claims 62-64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sha as applied to claim 59 above, and further in view of Endo.

63. As per claim 62-64, see discussion in claim 38-40.

Allowable Subject Matter

64. Claims 5-6, 9-11, 17-19, 36, 43, 48, 55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

65. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Examiner's note:

Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Prior Art not relied upon:

Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent T. Tran whose telephone number is (571) 272-7210. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas c. Lee can be reached on (57 1)272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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